Linear Threshold and SET based Logic devices, parameters and characteristics

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ABSTRACT

In business, engineering, science and technology, electronic goods of Low cost, low power consumption, high operating speed, and high integration density are economically requisite in the present era. Single electron based devices can be implemented in two ways (i) single-electron transistor (SET) and (ii) Threshold Logic gate(TLG). In this work the single electron devices are constructed using both (i) and (ii). TLGs as well as Single Electron tunneling devices (SEDs) have the power of managing /controlling the transport of an electron through a tunnel junction at a particular time when tunneling happens. A single electron containing the charge is sufficient to store one information in a SED. Power that is required in the single electron tunneling circuits is really low in comparison with the (CMOS) circuits. The processing delay is very low and speed of the processing of TLG based devices will be close to electronic speed. The single-electron transistor (SET) and TLG are attracting scientists, technologists and researchers to design and implement for the consuming of ultra-low power and their small sizes. When implementing any logic gate, any combinational as well as sequential circuit, TLG along with SET would be a best candidate to fulfill the requirements required for their implementations. So far as an Ultra-low noise is concerned, combination of TLG and SET based circuit can be treated as the best selection for implementing the desired circuits. Different gates like 2-input OR, 2-input AND, 3-input OR/NOR, 3-input AND/NAND, XOR/XNOR etc. have been implemented by using linear threshold logic gates. Truth table or simulated results of them are given in parallel in due places.

Key words: Oscillation, Electron-tunneling, Coulomb-blockade, linear threshold gate

1. INTRODUCTION

From the point of view of semiconductor technology that the ever decreasing feature size and the corresponding increase in density of transistors facilitates many improvements in semiconductor based designs. One day will come when such improvement will eventually come to an end. For ensuring further feature size reduction, possible imminent technologies with greater scaling potential like single electron tunneling technology is currently under the investigation of the researchers. Tunneling events happen when a single electron can pass through the tunnel junction under the action of bias voltage and multiple input voltages connected to the islands via small capacitors.

2. Structure of SET and Oscillation property

A SET consists of a source electrode connected to a tunnel junction having tunnel capacitance C_S and resistance R_S, a drain electrode connected to a tunnel junction having tunnel capacitance C_D and resistance R_D, a gate input voltage V_G joined to a true gate capacitance C_G which is capacitatively coupled with the island or quantum dot or simply dot (in Fig.1(a)). The island made up of gold is close to a spherical shape of diameter 10nm. The quantum dot may be controlled by a single gate electrode (Fig.1 (a)) or more gate electrodes (Fig.1 (b)). The transfer of an electron from the source to island or from island to drain or verse-visa is controlled by a voltage(s) connected to the gate electrode(s).

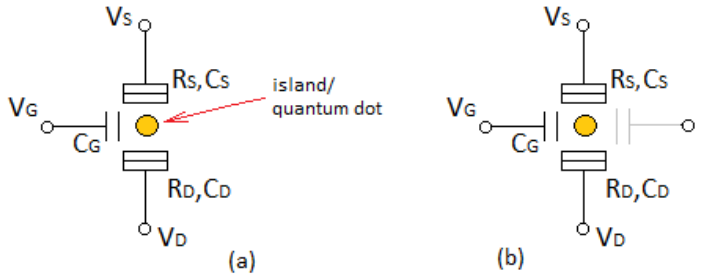


Fig.1 (a) A simple SET structure with one gate (b) with two gates

An electron can be entered into the island or ejected it from the drain depending upon the tunneling of that electron through a thin barrier of potential between the quantum dot and external electrode. We are to fulfill two conditions to observe the Coulomb-Blockade (CB) effect whether or not the tunneling happens.

(i) Whether there exists charge(s) on the quantum dot, we are to ensure that. Thermal fluctuations must not be able to add or subtract an extra single electron charge (e) in the dot. This means that the electrostatic charging energy, of course, will be much greater than thermal energy(K_BT), i.e., $\frac{E_C}{2C_\Sigma}>>(K_BT)$;

where C_Σ =sum of tunnel junction capacitances and true gate capacitance(s), T= *absolute* temperature, and Boltzmann's constant K_B=1.380649 × 10^{-23} J/K

(ii) Quantum fluctuations should be so low that the electron(s) can't move from the island. And this leads the tunnel junction resistances (R_S and R_D) to be greater than quantum resistance i.e., $R > \frac{h}{e^2} \cong 26K\Omega$, where Planck's constant h= 6.626 × 10^{-34} joule-seconds (J·s).

The two electrodes source and drain perform the oerations as of electron reserviors. The SET can be intentionally connected by an optional gate as shown in Fig.1 (b) (ritht side). This optional gate is set here only to tune the bias voltage V_{GS}. The gate electrode capacitatively coupled to the island allows the SET to shift the island energy level. So when the power is on for the SET the current passes through it. By altering the gate voltage the threshold voltage can be reduced or risen.The dependancy on threshold voltage of the this tunneling device(SET) is a periodic function having the periodic rate = $\frac{C_G}{e}$ or the period time = $\frac{e}{C_G}$. Whenever the gate electrode potential is enhanced to a certain lebel, electrons transit to the quantum dot. In the dot, the number of electrons is increased one by one according to the gate volktage is increased in sequence. Further, if gate voltage is enhanced, the electron number is increased as well. Noted that the periodicity of the drain-source current (I_{DS}) vs. gate voltage (V_{GS}) shownn in Fig. 2. The effect of Coulomb blockade happens at the maximum peak whenever the integer average quantity of electrons is staying on the quantum dot or island [1]. On the contrary, whenever a half-integer number of electron quantity residing on the island, there is no Coulomb blockade effect there. A (I_{DS}- V_{GS}) curve is depicted in the Fig. 2 for a SET showing the periodic oscillations defined as Coulomb Oscillations in the present situations.

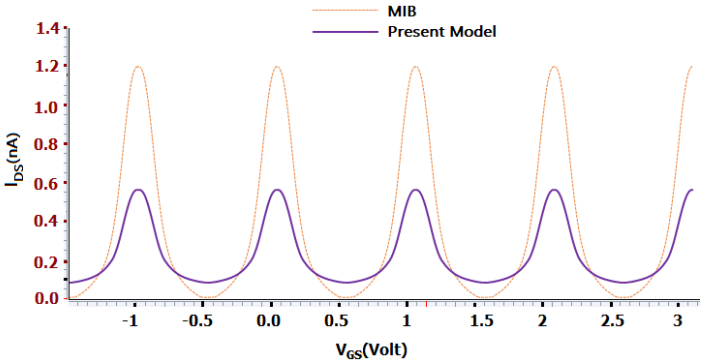


Fig. 2 At 300K Periodic Oscillations of I_{DS} vs. V_{GS}
when V_{DS}=120mv, C_G=0.23 aF, C_S=0.06aF,C_D=0.06aF

3. Operational temperature:

For the purpose of realization of atmospheric temperature operation called room-temperature operation, the device considered must be made up of much smaller in size. This size should be at such a level that enables a researcher to make useful as well as user-friendly circuits, rather than only performing the travelling phenomenon of an electron in conduction mode or in a Coulomb blockade condition. For some particular systems, the estimates have already been estimated for the process of constructing something very small using modern technology. Here we can provide an estimate about how far one can travel on a very rough but a complete common argument. The quantity of capacitance indeed needed in our interest. Capacitance between two conducting bodies we are considering has no lower limit, in principle. By placing these two particles far apart from each other, one can make the combined capacitance very small. But for tunneling purpose, a lower limit must exist for tunnel capacitance. Because, two conducting bodies should be in a close proximity for charged carriers to be tunneled between them. The combined capacitance relating to two small sized metal bodies (preferably gold) separated by distance L from each other is given by

$$\mathbf{C=4\pi\varepsilon_o \frac{r^2}{L}},$$

Accordingly, if the particles are being smaller and smaller, the capacitance between them goes towards that exists

between them irrespective of their sizes or shapes of those conducting particles/bodies. So, we can consider those two bodies as two spherical conductors as given in Fig. 3 below:

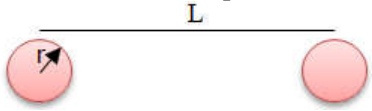


Fig.3 Two spherical conductors having radii *r*, separated by length *L*.

We take the radii of both the spherical metal are 'r' *each*. For making the mutual capacitance small, the length of radius 'r' *must* be as small as possible, and the separation 'L*'* *between* them must such a range so as to occur tunneling [2, 3]. The capacitance value, in a vacuum, for Fig. 3 is given by the equation (1),

$$\mathbf{C}=4\boldsymbol{\pi\varepsilon_o}\frac{r^2}{L}, \quad \text{Where, r<<L,} \cdots\cdots(1)$$

The value of $4\boldsymbol{\pi\varepsilon_o} \cong 1\times10^{-10}$F/m, taking the optimistic values r = 5 Å and L = 50 Å we have,

$$C=1\times10^{-10}\times\frac{5^2}{50}\times10^{-10}=0.5\times10\times10^{-20}=5\times10^{-21}\text{F}$$

If the dielectric constant $\boldsymbol{\varepsilon_o}$ is higher, the capacitance will be higher.
We should assume that the tunnel capacitance is very close to 0.1aF. Small capacitance close to this value is reported in [1, 2]. With this value the tunneling operation is possible at atmospheric temperature.

4. Current model SET

We are aware of "orthodox theory" of single electron tunneling, which makes us realize the physics of single electron devices like single electron transistor especially about the Coulomb blockade and Coulomb oscillations. This theory treats about the tunneling process as a simple sequential event ignoring the quantum nature of the tunneling process and other auxiliary effects like electron-phonon interaction. Under the condition of tunneling and Coulomb blockade, the tunneling rate of an electron through a potential barrier is given as

$$\Gamma(\Delta F)=\frac{\Delta F}{e^2R_T\ (1-\exp\left(\frac{-\Delta F}{K_BT}\right))} \cdots\cdots(2)$$

In this equation, R_T is being the tunnel resistance and ΔF indicates the free energy change. In SET theory, it does not give any information about statistics regarding the tunneling of many electrons at a time but the tunneling rate for a single electron. Considering that the states of tunneling and Coulomb blockade are discrete, then Master-Equation (ME) for SET models tries to find out the solution of equation (3) below.

$$\frac{\delta P_i(t)}{\delta t}=\sum_{i\neq j}[\Gamma_{ij}P_j(t)-\Gamma_{ji}P_i(t)] \cdots\cdots(3)$$

Here, Γ_{ij} is the transition rate starting from the state j to the state i, $P_i(t)$ is the probability of time-dependent occupancy of state i. In our SET based tunneling system, the tunneling resistances are considered to be constant for the purpose of providing quantitative description of current passing through the SET but ignoring some more physical effects relating to the SET, as the current and voltage concerning about the active mode of SET are verified and are compared with Monte-Carlo (MC) method With the help of Master-Equation (ME), the drain to source current I_{DS} is expressed as the function of tunneling rate (n) in equation (4) below.

$$I_{DS}=e\sum_{n=-\infty}^{n=\infty}P_n[\left(\vec{\Gamma}_S(n)+\overleftarrow{\Gamma}_D(n)\right)] \cdots\cdots(4)$$

Here, $\overrightarrow{\Gamma_S}(n)$ and $\overleftarrow{\Gamma_S}(n)$ represent tunneling rate from source to quantum dot and from quantum dot to source respectively with *n*-number of electrons on the quantum dot. For avoiding the complexity as to the drain to source current I_{DS} and for computing the time with near about the same accuracy, we must take the values of n as n = -2, -1, 0, 1 and 2. Whenever the equation (5) telling the characteristics of SET is discussed as the function of tunneling rates (n), we would be able to measure the current density against the barrier potential as a dependant function of internal attributes like operating temperature, energy level and junction characteristics.[19]

$$I_{DS}=e\times\frac{\begin{matrix}\left[\left(\vec{\Gamma}_S(-1)+\vec{\Gamma}_D(-1)\right)\left(\vec{\Gamma}_S(0)\right)+\vec{\Gamma}_D(0)\left(\vec{\Gamma}_S(1)+\vec{\Gamma}_D(1)\right)\right]+\left[\left(\vec{\Gamma}_S(0)+\vec{\Gamma}_D(0)\right)\left(\vec{\Gamma}_S(-1)-\vec{\Gamma}_S(-1)\right)+\left(\vec{\Gamma}_S(1)+\vec{\Gamma}_D(1)\right)\right]+\\ [\left(\vec{\Gamma}_S(0)+\vec{\Gamma}_S(0)\right)\left(\vec{\Gamma}_S(1)+\vec{\Gamma}_D(1)\right)\vec{\Gamma}_S(-1)\left(\vec{\Gamma}_S(1)-\vec{\Gamma}_S(1)\right)\left(\vec{\Gamma}_S(0)+\vec{\Gamma}_S(0)\right)\left(\vec{\Gamma}_S(1)+\vec{\Gamma}_D(1)\right)\vec{\Gamma}_S(-1)]\end{matrix}}{\begin{matrix}[\frac{\left(\vec{\Gamma}_S(-1)+\vec{\Gamma}_D(-1)\right)\left(\vec{\Gamma}_S(0)\right)+\vec{\Gamma}_D(0)\left(\vec{\Gamma}_S(1)+\vec{\Gamma}_D(1)\right)}{\vec{\Gamma}_S(-2)}+\frac{\left(\vec{\Gamma}_S(1)+\vec{\Gamma}_D(1)\right)\left(\vec{\Gamma}_S(0)+\vec{\Gamma}_D(0)\right)\vec{\Gamma}_S(-1)}{\vec{\Gamma}_D(2)}]\\ +[(\vec{\Gamma}_S(0)+\vec{\Gamma}_S(0))\left(\vec{\Gamma}_S(1)+\vec{\Gamma}_S(1)\right)+(\vec{\Gamma}_S(0)+\vec{\Gamma}_D(0))\vec{\Gamma}_S(-1)+(\vec{\Gamma}_S(1)+\vec{\Gamma}_D(1))\vec{\Gamma}_S(-1)]\end{matrix}} \cdots\cdots(5)$$

We should calculate the resistance function of bias voltage and add this value to the the equation (5). At the extreme level of atmospheric temperature, electron becomes excited beyond the potential barrier and they freely move there and create a channel in parallel to the tunnneling channel through the SET. In this situation, it wouild be better to get some knowledge regarding thermoionic emission from SET. This thermoionic emission R_{Th-io} can be calculated by using the expression (6).

$$R_{Th-io}=A\times T^2 exp\left(\frac{-e(\varphi_0-\sqrt{\frac{eE}{4\pi\varepsilon_r\varepsilon_0}})}{K_BT}\right)\ldots\ldots\ldots\ldots\ldots\ldots(6)$$

In this expression A= Richardson constant, φ_0 = the barrier potential height, E=electric field, ε_0= space permittivity, ε_r=dielectric constant

Therefore the total current i.e., sum of tunneling current and thermal current due to high temperature effect represented in the Fig. 4.

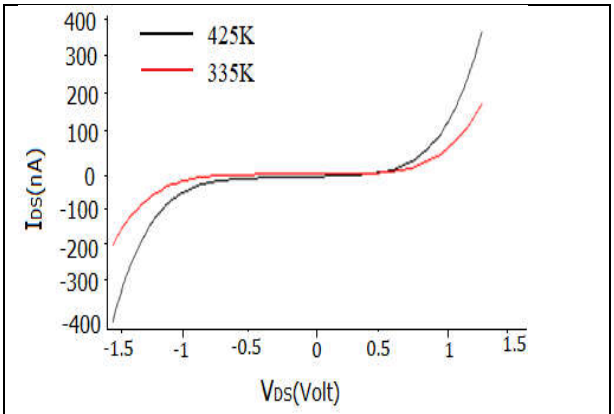


Fig. 4 Current Vs. Voltage curve when V_{GS}=0 at different temperatures at 300K and 335K .The values of C_G=21aF, $C_G = C_G = 0{,}06aF$ are taken here.

5. NOT gate or INVERTER or COMPLEMENT

The buffer or inverter [5, 6, 7, 11, 13] depicted in Fig. 2(a) is made up of two single electron transistors (SETs) connected in series. The two input voltages having the same values are directly coupled to the islands of the SET1 and SET2 [9, 10] through two capacitors C_1 and C_2 of same values respectively. The islands of each SETs have a size close to 10 nm diameter of gold and their capacitances should be less than 10^{-17} F. The output terminal $V_0$is connected to the common channel between SET1 and SET2 and to the ground through a capacitor C_L to put down charging effects.

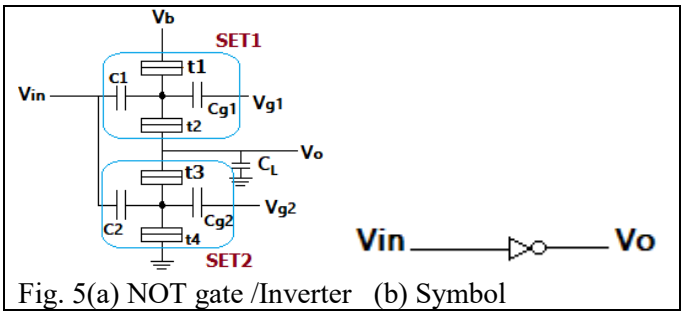
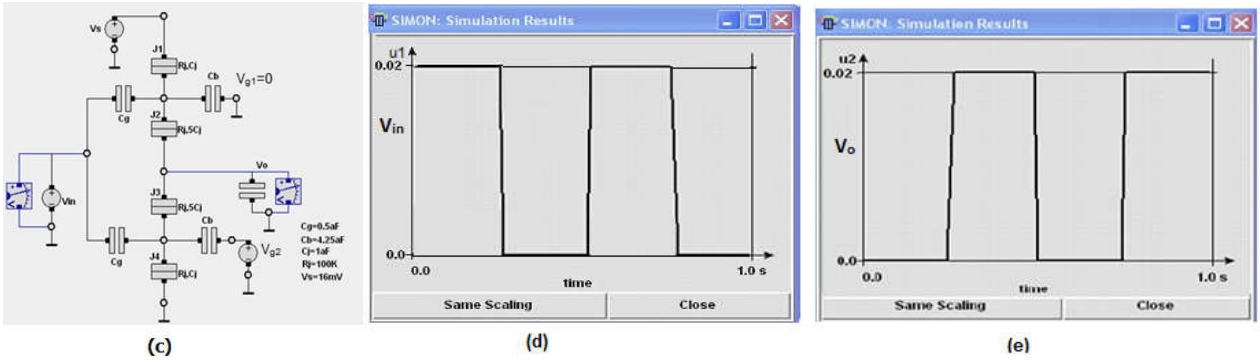


Fig. 5(a) NOT gate /Inverter (b) Symbol

For the buffer, the parameter values chosen are:V_{g1}=0, V_{g2}=0.1× $\frac{q_e}{C}$, $C_L = 9C$, $t_4 = \frac{1}{10}C$, $t_3 = \frac{1}{2}C$, $t_2 = \frac{1}{2}C$, $t_1 = \frac{1}{10}C$, $C_1 = \frac{1}{2}C$,$C_2 = \frac{1}{2}C$,$C_{g1} = \frac{17}{4}C$ and $C_{g2} = \frac{17}{4}C$, R1 =R2=50KΩ. From the point of view of simulation purpose we adopt C = 1aF.



(c) (d) (e)

Fig. 5(c) Simulation set of NOT gate; Simulation result of NOT (d) input (e) output

The operation of the inverter will be described as: - the output V_0 value will be high in case the input voltage V_{in} is low and the V_0value will be low in case the input voltage is high. To achieve this target, we must set the voltages for $V_{g1} = 0$ *and* V_{g2}=16mV along with the tuning gate voltages, at present, V_{in} both for SET1 and SET2. SET1 is in conduction mode if V_{in} is set to low and the SET2 is in Coulomb blockade [5-7, 16, 19, 20].

This combination provides the output voltage V_0 connected to V_b as a result the output shows high. Coulomb blockade phenomenon breaks the steady flow of current, whenever the high input (logic 1) is switched on at the input terminal(s), it makes the immediate shift of induced charge on both of the islands or quantum dots of the two SETs by a fraction of an electron charge and enforces the SET1 in Coulomb blockade and the SET2 in conducting mode. As a result, the output alters from high state to low (or logic 0).

In this work, the logic inputs "0" =0 Volts and logic "1"=0.1× $\frac{q_e}{C}$.

For simulation and other purposes, will consider that C=1aF and Logic "1"= 0.1× $\frac{1.602\times10^{-19}}{1\times10^{-18}}$=0.1 × 1.602 × 10^{-2}=16.02 × 10^{-3} =16.02 ≅ 16 mV.

6. LOGIC GATES A ND LINEAR SEPARATION

Before discussing about different threshold logic gates, one should be known about linear condition of a function. We are trying to make understand how shall we comment about a linear or non-linear function? Now we will observe how the basic gates for two inputs variables x1 and x2 are implemented for the input space by linear separation. The solution spaces functions of gates for four gates AND, OR, NOR and XOR in Fig. 6 bearing four vertices each and they are represented by 00, 01, 11 and 10. We point them as red circle-points having the function value=1, and the yellow colored small circle points having value = 0(zero).

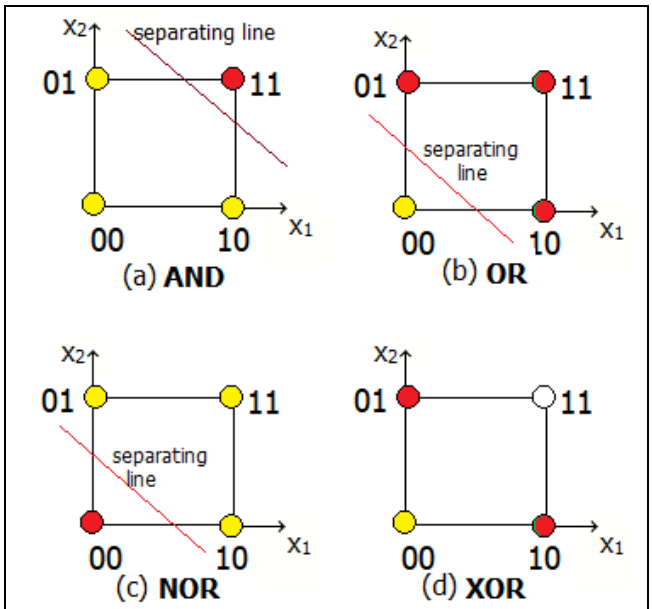


Fig. 6 Solution spaces of x1 and x2 (variables) for (a) AND, (b) OR , (c) NOR and (d) XOR gates

In Fig.6 (a) and 6(b) and 6(c), we have drawn one straight line, called separating line, for each diagram to separate 0-vertices by1-vertices. As it follows the linearly separable conditions so we will be able to implement the functions AND, OR and NOR by a single neuron. This is not true for XOR/(XNOR) in Fig. 6(d), since no line can separate the 1-vertices of XOR function from its 0-vertices. So, XOR is not being a linearly separable function. In two dimensions, a line separates points in a plane, whereas a plane is considered as a separator of points in three dimensional spaces. An (n-1) dimensional plane (we call it a hyper plane) is considered to be a separator for points in n-dimensions, in general. For example, if a separator is of two dimensional it can separate a three dimensional space. We are trying to clarify regarding linearly separable cases through the three examples given below.

Definition 1: A switching function can be treated as linearly separable when all its related 1-vertices are kept separated by all of its 0-vertices by using a hyper plane. A neuron bearing $n-inputs$works on $an\ n-dimensional$ space and a single neuron which is capable of implementing any switching function is thought to be linearly separable.

Example1:

A single neuron can implement a switching function $f(x_1,x_2,x_3)$=x_1+x_2x_3 +x_1x_2, since its1–vertices can't be separated from 0-vertices by a plane as shown in Fig. 7 and the related truth table is given below in Table-1.

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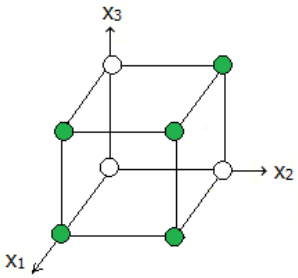


Fig. 7 Space for $f(x_1,x_2,x_3)$, a non-linear threshold logic function

Table-1

x_1	x_2	x_3	f(x_1,x_2,x_3)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Example2:

A single neuron can implement a switching function $f(x_1,x_2,x_3)$=x_1 + x_2+$\bar{x}_2x_3$, since its 1-vertices can be separated from all 0-vertices by a plane as shown in Fig. 8 and its truth table is shown in Table-2.

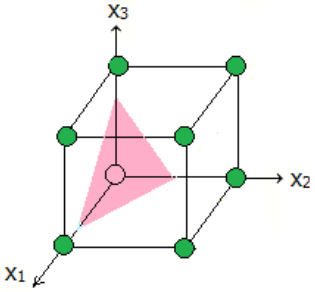


Fig. 8 Space diagram with a hyper plane of linear threshold logic function

Table-2
Truth table of $x_1 + x_2 + \bar{x}_2 x_3$

x_1	x_2	x_3	$f(x_1, x_2, x_3)$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Example3:
A single neuron can implement a switching function $f(x_1, x_2, x_3) = x_1 x_3 + x_2 \bar{x}_3$, since its 1–vertices can be separated from all 0-vertices as shown by a separating line in Fig. 9 and related truth table is given below in Table-3.

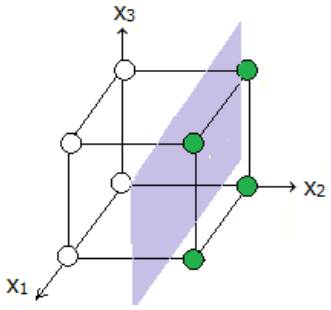


Table-3
Truth table of $x_1 x_3 + x_2 \bar{x_3}$

x_1	x_2	x_3	f(x_1, x_2, x_3)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Fig. 9 Space diagram with a hyper plane of linear threshold logic function

7. General Concept of Threshold in Multi-in single-out

A threshold logic gate of Multi-in and single-out [3-7, 12-13] shown in Fig. 9a is made up of a tunnel junction having capacitance C_j and resistance R_j, two multiple input-signals V_k^Ps and V_l^ns connected at two points 'q' and 'p'. Where each input voltage V_k^P is connected to the point "q" through their corresponding capacitors $C_k^P s$; and each input voltage V_l^n, is connected to the point "p" through their respective capacitors C_l^ns. The supply voltage or bias voltage V_b is connected to the point"q" through a capacitor C_b also. Junction capacitor C_j is connected to point "p" which is connected to the ground through capacitor C_0. LTGs can be implemented with the help of a function presented by the signun function of h(x) expressed by equations (6a) and (6b).

$$g(x) = \text{sgn}\{h(x)\} = \begin{cases} 0, & if\ h(x) < 0 \\ 1, & if\ h(x) \geq 0 \end{cases} \quad \text{(6a)}$$

$$h(x) = \sum_{k=1}^{n} (w_k \times x_k) - \theta \quad \text{(6b)}$$

where x_k being the n-Boolean inputs and w_k being their corresponding n integer weights.

The LTG compares the weighted sum of the inputs $\sum_{k=1}^{n} (w_k \times x_k)$ with the threshold value θ.When the weighted sum-value is greater than or equal to the critical voltage or threshold value θ then the logic output of the LTG will be high (logical "1"), otherwise it refers to a low (logical "0").

Two basic circuit elements in a LTG being the tunnel junction capacitance C_j and the capacitance C_0 are connected in series. The input signal voltages $V_1^P, V_2^P, V_3^P, \ldots, V_k^P$, which are weighted by their corresponding vector capacitances $C_1^P, C_2^P, C_3^P, \ldots, C_k^P$, are added to the junction voltage, V_j. In contrast, the input signal voltages $V_1^n, V_2^n, V_3^n, \ldots, V_l^n$ weighted by their corresponding vector capacitances $C_1^n, C_2^n, C_3^n, \ldots, C_l^n$, are being subtracted from the voltage, V_j.

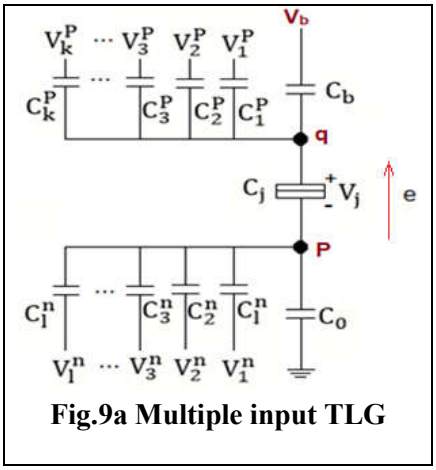


Fig.9a Multiple input TLG

The critical voltage V_c is indeed required to enable tunneling action, and which acts as the intrinsic threshold of the tunnel junction circuit. The supply or bias voltage V_b connected to tunnel junction through the capacitance, C_b, is being used to adjust the gate threshold to the desired value θ. A tunneling event happens though the tunnel junction, only when an electron passes through the junction from p to q as directed by a green arrow in Fig. 9a.
The following notations we will use for the rest our discussion.

$$C_\Sigma^P = C_b + \sum_{k=1}^{g} C_k^P \quad \text{(6c)}$$

$$C_\Sigma^n = C_0 + \sum_{l=1}^{h} C_l^n \quad \text{(6d)}$$

$$C_T = C_\Sigma^P C_j + C_\Sigma^P C_\Sigma^n + C_j C_\Sigma^n \quad \text{(6e)}$$

Whenever all voltage sources in Fig. 9a are connected to ground, the circuit can be thought of as it is made up of three capacitors namely, C_Σ^P, C_Σ^n and C_j, connected in series. C_T is taken to be the sum of all 2-term products of these three capacitances C_Σ^P, C_Σ^n and C_j.
Now we are to find out the expression as to the critical voltage V_c of the tunnel junction. We may take the capacitances of the whole circuit as: (i) the capacitance of the tunnel junction to be C_j and (ii) the remaining part of the circuit has the equivalent capacitance to C_e, as observed from the point of view of tunnel junction; we can measure the threshold or critical voltage [3-6, 12-13] for the tunnel junction as below.

$$V_c = \frac{e}{2(C_j + C_e)} \quad \text{(6f)}$$

$$= \frac{e}{2[C_j + (C_\Sigma^P || C_\Sigma^n)]}$$

$$= \frac{e}{2[C_j + \frac{(C_\Sigma^P)*(C_\Sigma^n)}{(C_\Sigma^P + C_\Sigma^n)}]}$$

$$= \frac{e(C_\Sigma^P + C_\Sigma^n)}{2[C_j * (C_\Sigma^P + C_\Sigma^n) + (C_\Sigma^P) * (C_\Sigma^n)]}$$

$$= \frac{e(C_\Sigma^P + C_\Sigma^n)}{2C_T} \quad \text{(6g)}$$

Given that the voltage of the junction is V_j, a tunneling event comes to happen through this tunnel junction if and only if the condition given below is satisfied.

$$|V_j| \geq V_c \quad \text{(6h)}$$

It is decided that if the junction voltage is less than the critical voltage i.e. $|V_j| < V_c$, then there will be no tunneling event through the tunnel junction. As a consequence, the tunneling circuit remains in a *stable state*.
We can also write for the function h(x) as [12-13]

$$C_T h(x) = C_\Sigma^n \sum_{k=1}^{g} C_k^P V_k^P - C_\Sigma^p \sum_{l=1}^{h} C_l^n V_l^n - 0.5(C_\Sigma^P + C_\Sigma^n)e + C_\Sigma^n C_b V_b \quad \text{(6g)}$$

$$h(x) = C_\Sigma^n \sum_{k=1}^{g} C_k^P V_k^P - C_\Sigma^p \sum_{l=1}^{h} C_l^n V_l^n - \theta \quad \text{(6h)}$$

$$\text{and} \quad \theta = 0.5(C_\Sigma^P + C_\Sigma^n)e - C_\Sigma^n C_b V_b \quad \text{(6j)}$$

8. Threshold logic equation for OR gate

In general, we assume that the threshold logic equation for OR gate is F(A,B)= sgn$\{w_A.A + w_B.B - \theta\}$.To make the threshold logic OR gate, we draw the Table-4 of OR gate and compare the weights w_A and w_B of two variables A and B respectively with the threshold value θ.

Table-4

A	B	F(A,B)	θ	Eqn. no.
0	0	0	$0<\theta$	(1)
0	1	1	$w_B \geq \theta$	(2)
1	0	1	$w_A \geq \theta$	(3)
1	1	1	$w_B + w_A \geq \theta$	(4)

For the 4 equations in Table-4, if we assume w_B=1, w_A=1 and θ=0.5, then all the 4 equations are satisfied. Hence the Threshold logic equation for OR gate is given in equation (7) and its corresponding threshold logic gate is drawn in Fig. 10(a)

$$OR(A,B) = sgn\{A + B - 0.5\} \cdots\cdots (7)$$

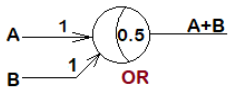
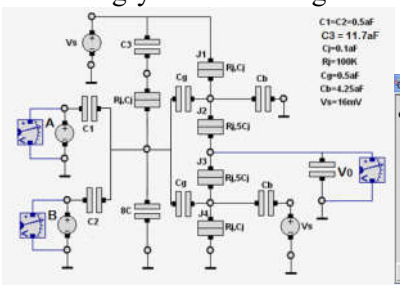


Fig. 10(a) Threshold logic OR gate

For implementing the OR gate we shall use the parameters$C_1^n = C_2^n$=0.5aF,$C_3 = 11.7aF, C_{b1} = C_{b2} = 4.25aF$, $C_{g1} = C_{g2} = 0.5aF, C_L = 9aF, C_0 = 8aF$, R_j=$10^5\Omega$, $V_s = 16mV$ in Fig. 10(a) and accordingly after running the simulator the output we get is given in Fig. 10(b)-(e).



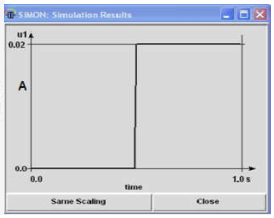
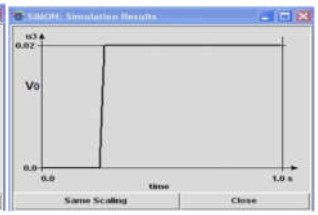


Fig. 10(b) OR gate (c)



(d) (e)

Fig. 10(c)-(e) simulation result of OR gate

9. For the case of NOR

It is well-known that an Inverter inverts itself, i.e. it complements its own input signal, Now we shall modify the threshold equation of OR(A,B) in section 8 so that it create NOR(A,B). So when we combine the result of OR(A,B) with a buffer or inverter, a new threshold logic buffered gate, we get, that gives us the value of NOR (A, B) and the equation of the NOR logic gate will be

NOR (A, B) =$\overline{OR(A,B)}$

$$= sgn\{-A - B - (-0.5)\} \cdots\cdots (8)$$

Here the value of the threshold voltage -0.5 may be any value in the range of $-1 > \theta \geq 0$.

Table-5

A	B	$\{W_A + W_B\}$	$\theta = -0.5$	$F(A,B)$
0	0	0	$0 \geq -0.5$	1
0	1	-1	$-1 < -0.5$	0
1	0	-1	$-1 < -0.5$	0
1	1	-2	$-2 < -0.5$	0

From the Table -5 it is observed that F (A, B) satisfies all the conditions of an NOR gate, so the equation (8) we have is correct. Simulation set and simulation result are given in Fig, 11(a) and 11(b) respectively.

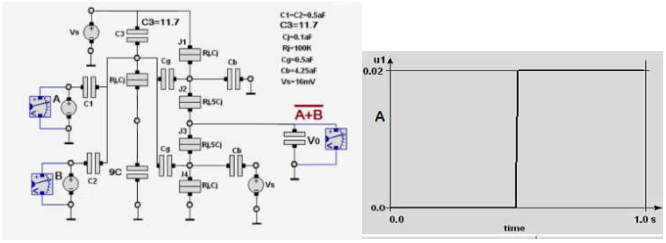
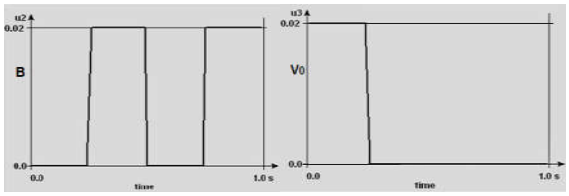


Fig 11(a) TLG based NOR gate



Fig, 11(b) Simulation result of NOR gate

For implementing the buffered Boolean logic NOR gate we will use the parameters logic input "0"=0V, logic "1" = 16mV, $C_1^n = C_2^n$=0.5aF,$C_3 = 11.7aF, C_b = C_{b1} = C_{b2} = 4.25aF, C_{g1} = C_{g2}$ =0.5aF, $C_L = 9aF, C_0 = 9aF$, $R_j = 10^5\Omega, V_s = V_b$ =16mVand accordingly after simulation the result we have is given in Fig. 6(b).

10. 2-input AND gate

For making the threshold logic gate of 2-input AND gate, we can draw the Table-6 of an AND gate and compare the weights of variables w_A and w_B of two variables A and B respectively with the threshold θ $[3-7]$.

Table-6

A	B	F(A,B)	θ	Eqn. no.
0	0	0	0<θ	(1)
0	1	0	$w_B < \theta$	(2)
1	0	0	$w_A < \theta$	(3)
1	1	1	$w_B + w_A \geq \theta$	(4)

After solving the 4 equations in 4th column of Table 6, we get one set of solution w_B=1, w_A=1 and θ=2. So the Threshold logic equation for AND gate is given in equation (9) and its corresponding threshold logic gate is drawn in Fig. 12(a)

$AND(A,B) = sgn\{A + B - 2\}$ ..... (9)

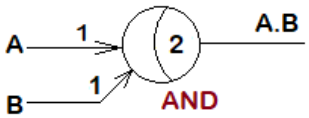


Fig. 12(a) Threshold logic AND gate

For implementing the AND gate we will use the parameters $C_1^n = C_2^n = 0.5aF, C_{b1} = C_{b2} = 4.25aF, C_{g1} = C_{g2} = 0.5aF, C_L = 9aF, C_0 = 8aF$, $R_j = 10^5\Omega$.The simulation set is given in Fig. 12(b) and after simulating the result we get is given in Fig. 12(c).

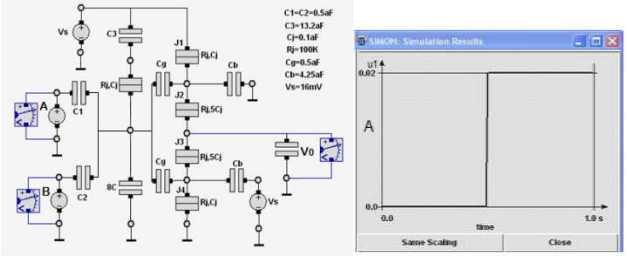
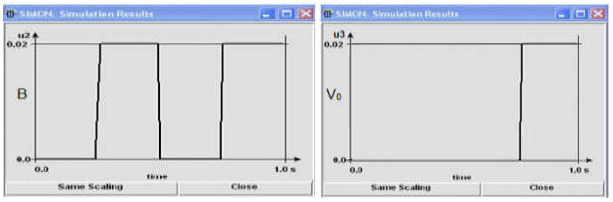


Fig.12 (b) AND Gate (c)



(d) (e)

Fig.12 (d), (e) Simulation result of 2-input AND gate

11. Threshold logic equation for 3-input AND gate and 3-in NAND gate

As AND gate is a positive logic we shall assume that all the values of w_A, w_B, w_C andθ are positive. If we take $w_A = 1, w_B = 1, w_C$=1 and $\theta = 2.5$ (or any value in the range $2 < \theta \leq 3$), then all the conditional equations in the 5th column in Table-7 are satisfied. So the threshold logic equation for 3-input AND gate is

$AND(A,B,C) = sgn\{A + B + C - 2.5\}$ ..... (10)

Table-7

A	B	C	F(A,B,C)= ABC	θ
0	0	0	0	$0<\theta$
0	0	1	0	$\theta > w_C$
0	1	0	0	$\theta > w_B$
0	1	1	0	$\theta > w_B + w_C$
1	0	0	0	$\theta > w_A$
1	0	1	0	$\theta > w_A + w_C$
1	1	0	0	$\theta > w_A + w_B$
1	1	1	1	$w_A + w_B + w_C \geq \theta$

In the same way, we can obtain a solution set for 3-input NAND gate, $w_A = -1$, $w_B = -1, w_C = -1$ and $\theta = -2.5$. So, the corresponding threshold logic gate will be

NAND (A,B,C) $= sgn\{-A - B - C - (-2.5)\}$ ..... (11)

Simulation arrangement and active simulation result are shown in Fig. (13a) and 13(b) below.

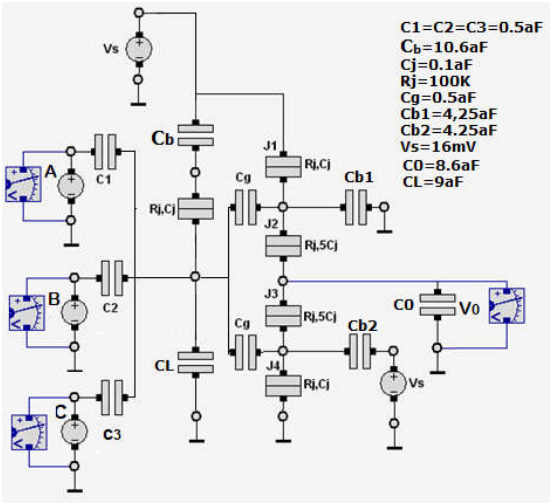
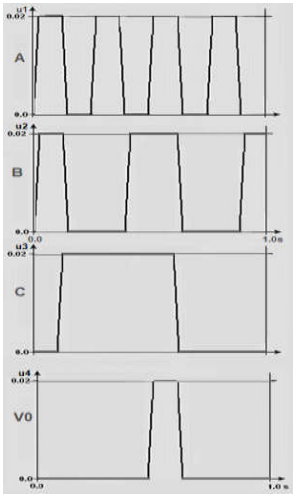


Fig. 13(a) Simulation set of 3-input AND gate



(b) Simulation result of 3-input AND gate

As stated earlier, the threshold gates those are derived from the generic threshold gate given in Fig.9a require an output buffer for the correct operation in a network structure. It is well-known that the applied buffer inverts its own input signal, we modify the threshold equation of $AND(A,B,C)$ such that it determines NAND(A,B,C) = $\overline{\text{AND(A,B,C)}}$. So when we combine the result of $\overline{\text{AND(A,B,C)}}$ and a buffer in series, a buffered gate obtained calculates $AND(A,B,C)$. Truth table of 3-input NAND gate and the threshold relationships with the weighted sum is given in Table-8.

$$\text{NAND}=\overline{\text{AND(A,B,C)}}=sgn\{-A - B - C + 2.5\}$$
$$=sgn\{-A - B - C - (-2.5)\} \text{ ..... (12)}$$

Table-8
Truth table of Threshold NAND gate

A	B	C	$\{w_A + w_B + w_C\}$	$\theta = -2.5$	F(A,B,C) $= \overline{ABC}$
0	0	0	0	$0 > -2.5$	1
0	0	1	-1	$-1 \geq -2.5$	1
0	1	0	-1	$-1 \geq -2.5$	1
0	1	1	-2	$-2 \geq -2.5$	1
1	0	0	-1	$-1 \geq -2.5$	1
1	0	1	-2	$-2 \geq -2.5$	1
1	1	0	-2	$-2 \geq -2.5$	1
1	1	1	-3	$-3 < -2.5$	0

From the Table-8, it is transparent that equation (12) acts as the equation of a 3-input NAND gate. As a consequence, when we combine this NAND gate and the buffer in series, a 3-input AND gate creates and provides correct output.

12. XOR Gate

The logic function of XOR gate is defined as Y=A.$\bar{B}$ +$\bar{A}$.B, where A and B are two variables. Space plot diagram of Y in 2D space is shown in Fig. 14(c). From this, we observe that no linear separating line that is separating the green and colorless bubbles can be drawn. So, one can decide that the Boolean logic function is not linearly separable. Therefore we would not be able to draw a threshold logic gate that represents the equation Y=A.$\bar{B}$ +$\bar{A}$.B.

To express Y=A.$\bar{B}$ +$\bar{A}$.B by a TLG, we firstly express P = (A.$\bar{B}$) by threshold gate-based equation as in equation (13) below.

P = $sgn\{A + \bar{B} - 2\}$ ..... (13)

As we know B + $\bar{B}$ =1 or $\bar{B}$= − B + 1, the equation (13) can be written as equation (14).

P = $sgn\{A - B - (1)\}$ ..... (14)

According to equation (14), we have drawn a threshold gate of P = A.$\bar{B}$ in Fig 14(a). Using two buffers in series with Fig. 14(a) we get the Fig. 14(b) which provides the same result as does the Fig.14 (a).

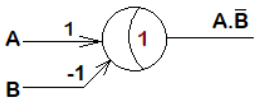
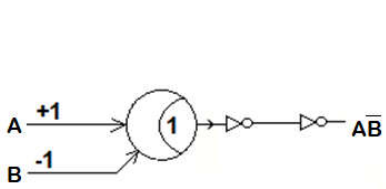


Fig. 14(a) Threshold gate of P = A.B



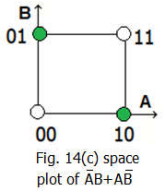


Fig. 14(c) space plot of $\bar{A}B+A\bar{B}$

Fig. 14(b) Threshold gate of A.$\bar{B}$ using 2-buffers/NOTs

Truth Table of equation P = (A.$\bar{B}$) is given in Table-9.

Table-9

A	B	$\bar{B}$	P
0	0	1	0
0	1	0	0
1	0	1	1
1	1	0	0

We can modify the threshold equation of P as we know that the buffer inverts its input signal, so it calculates $\bar{P}$=$\bar{A}$+B or $\bar{P}$=sgn $\{-A+B-(-0.5)\}$ and its corresponding truth table is given in Table-10.

Table-10

Truth table of $\bar{P}$

A	B	$\bar{P}$	θ = -0.5
0	0	1	0 ≥ θ
0	1	1	$w_b \geq \theta$
1	0	0	$w_a < \theta$
1	1	1	$w_a + w_b \geq \theta$

For implementing the threshold logic gate of $\bar{P}$ we require the logic input "0"=0V, logic "1" = 16mV, C=1aF, $C_1^n = C_1^P = \frac{1}{2}C$ =0.5aF, $C_b = 10.24aF$, $C_j = 0.25aF$, $C_L = 9aF, C_0 = 9.5aF$, R_j=$10^5\Omega$,. $V_b = 0.95\, e/C = 15.2mV$ $(as\ e/C = 160mV)$ which is close to 16mV, so V_b =V_s=16mV.

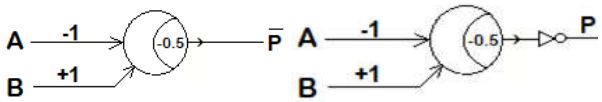


Fig. 15 (a) Threshold logic gate of $\bar{P}$ (b) of P

The Boolean expression Y=A.$\bar{B}$ +$\bar{A}$.B is to be expressed in another form by assuming P=$\bar{A}$.B, So Y = P + $\bar{A}$.B.

$Y = P + \bar{A}.B$ ..... (15)

For finding out the threshold gate logic of equation (15), we draw the truth Table-11 with the assistance of Table-9, and from Table-10 we solve the equations to get the weight values in 5th col. of Table-11.

Table-11

A	B	P	Y	θ
0	0	0	0	$0<\theta$
0	1	0	1	$W_2 \geq \theta$
1	0	1	1	$W_1 + W_3 \geq \theta$
1	1	0	0	$W_1 + W_2 < \theta$

After solving the conditional equations in Table-11, we obtain a solution set $\{W_1, W_2, W_3; \theta\}$ = {-1, 1, 2 ; 1}.

Hence the Threshold equation for the Y or an for XOR is

Y = sgn$\{-A + B + 2P - (1)\}$ ..... (16)

And its corresponding Threshold logic gate is depicted in Fig. 16**.** For correct operation, we are to apply a buffer in series to obtain an XNOR which is also shown in Fig. 16. If we again add another buffer in series we obtain an XOR gate shown in Fig. 16 as well.

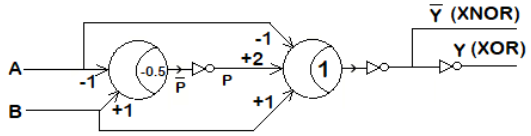


Fig. 16 XOR/ XNOR gate of two inputs

13. Discussion

We have discussed about different logic gates and a converter based on the LTG gates. We are to observe about their speed which is slow or fast. We are intended to find out the processing delay of a logic gate. In this situation we should include two parameters like: (i) the critical voltage $V_c$and (ii) tunnel junction capacitance C_j.However, assuming the atmosphere temperature at $T = 0K$, the switching/processing delay of a logic gate can be calculated with the help of the approaches [11-12].

Delay = $-(e|\ln(P_{error})|R_t) / (|V_j| - V_c)$ ..... (17)

Where, junction voltage =V_j, critical threshold voltage=$V_c$and being the junction resistance = R_t.

The switching will happen whenever the critical voltage V_c has the value less than the tunnel junction voltage V_j, i.e., $V_c < |V_j|$, but very near to it.This happens when V_{in1} is logic 1, resulting V_j =11.8mV for the case of a 2-input NOR gate in Fig-11(a), the critical voltage of the tunnel junction voltage V_c is 11.58mV. Given that the probability of error change P_{error} =10^{-12} and tunnel resistsnce $R_t = 10^5\Omega$. After calculation we get a gate delay equal to 0.07281$|\ln(P_{error})|$ns = 1.675 ns. In this manner, we can calculate the circuit delays written in Table-12.

Whenever an electron passes through the tunnel junction, the amount of total energy in the circuit changes after the tunneling events. The difference between the energy levels before and after the tunneling event is found to be

$$\Delta E = E_{before\ tunnel} - E_{after\ tunnel}$$
$$= -e(V_c - |V_j|) \cdots\cdots\cdots\cdots\cdots\cdots (18)$$

and it is the amount of switching energy being consumed when a tunnel event occurs in the tunneling circuit. We have drawn curves as to the switching delay as a function of the switching error probability in Fig. 17(a) and the switching delay as a function of the unit capacitance C shown in Fig. 17(b). Switching power vs. gate(element) is given in Fig. 17(c).

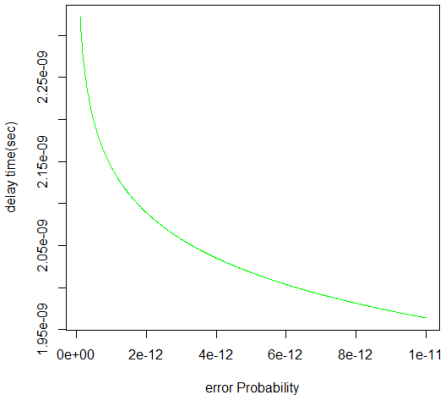


Fig. 17(a) Delay vs. Error Probability

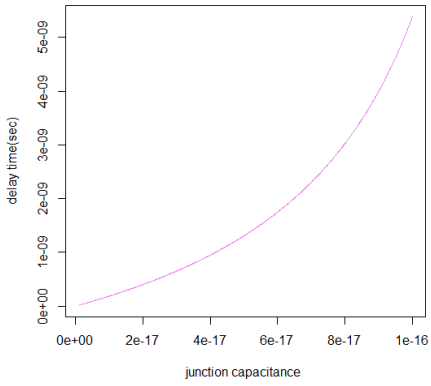


Fig. 17(b) Delay Vs. capacitance

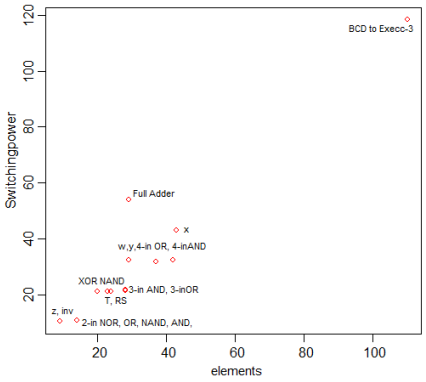


Fig. 17(c) Switching energy vs. elements

We have counted the element numbers for each and every case of gates or circuits, their switching delays, and switching energy consumptions for the corresponding LTGs (using the same methodology as adopted for the Boolean gates). All the calculated parameters are shown in tabular form in Table-12. Time delays for SET and LTG for different gates are shown Table-13.The relative time delays for different gates with respect to SET and LTG is given in Fig. 18.

Table-12

Gate/Device	elements	Delay	Switching Energy
inverter	09 elements	0.022|ln(P_{error}) | ns	10.4 meV
2-input NOR	14 elements	0.072|ln(P_{error})| ns	10.7 meV
2-input OR	14 elements	0.062|ln(P_{error})| ns	10.8 meV
2-input NAND	14 elements	0.080|ln(P_{error}) |ns	10.7 meV
2-input AND	14 elements	0.062|ln(P_{error}) |ns	10.8 meV
3-input AND	28 elements	0.104|ln(P_{error}) | ns	21.6 meV
3-input NAND	28 elements	0.072|ln(P_{error}) | ns	21.4 meV
2-input XOR	20 elements	0.102|ln(P_{error})| ns	21.2 meV
3-input OR	28 elements	0.104|ln(P_{error}) | ns	21.6 meV
4-input OR	42 elements	0.104|ln(P_{error}) | ns	32.4 meV
4-input AND	42 elements	0.104|ln(P_{error}) | ns	32.4 meV

The processing delays vary from one logic gate or circuit to other. If we take a 3-input AND gate we find its switching delay 0.104|ln(P_{error})| ns, similarly for a 2-input AND gate it is 0.062|ln(P_{error}) | ns, and so on. Given that the value of P_{error} equals to 10^{-12}, so the time after which the 1st output of the 2-input XOR gate will fan out is 0.102|ln(P_{error})| ns =2.81ns. i.e., after every 2.81ns, the next output bit will be taken from the counter. Therefore clock time/duration of the clock signal should be more than or equal to 2.81ns provided synchronization is essential. In this situation, the speed of the XOR gate will be $(1/2.81)ns$ = 0.3558 GHz =3.55× 10^8Hz.

We are interested in comparing the circuit delays of CMOS, SET-based and LTG-based. The processing delay or switching delay for a CMOS logic gate like AND, NAND, NOR, XOR is 12ns [21, 22], on the other hand the time required for tunneling through a single electron transistor (SET) [9-10] is approximately 4ns [5-8, 21-22].

Table-13
Switching delays of SET and LTG

Gate/Device	SET-based delay	LTG-based delay
inverter	8	0.60ns
2-input NOR	4	1.67ns
2-input OR	4	1.71ns
2-input NAND	4	2.21ns
2-input AND	4	1.71ns
3-input AND	8	2.87ns
3-input NAND	8	1.98ns
2-input XOR	4	2.81ns
3-input OR	8	2.87ns
4-input OR	12	2.87ns
4-input AND	12	2.87ns

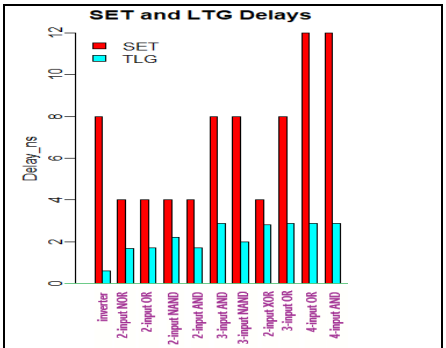


Fig.18 Delay comparison of SET and LTG

The XOR gate using conventional logic circuits needs 16 transistors, whereas the same function can be implemented with the help of 2 TLGs and 2 buffers/ NOT gate [3-8, 11,13] i.e. we will be able to reduce the number of nodes from 16 to 2.

14. Conclusion

The structure of a "One-electron-tunneling based transistor" also called "single electron transistor" and its oscillation property is discussed in section 2**.** In section 3, we have discussed about the temperature dependency for the operation of SET. In section 4, a concept regarding the current from source to drain is given. Next, how an electron passes through an inverter made from SET is discussed. Then, we have been able to construct a TLG using a generic Linear Threshold logic concept, and based on this TLG some members of logic family as OR, AND, NAND, XOR etc are implemented. All such gates have been verified by means of simulation using SIMON and their corresponding output waveforms are provided in due places. Comparing SET based device, it is observed that TLG based gates/ circuits are more than two times faster than single electron transistor based logic circuits.
At the time of operation, we must take care of maintaining the atmospheric temperature close to (0-1) K.

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