# Designing and Implementation of BEC-1 using Reversible logic gate in QCA Technology

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***Abstract*— Quantum-dot cellular automata is an ideal computational model that offers lowered size, reduced energy consumption, higher speed, and deliberate design at nanometer scale. It was created as a solution to the scalability issue inherent in conventional Complementary Metal Oxide Semiconductor technologies. Coulomb repulsion is the foundation upon which the revolutionary nanotechnology known as QCA is built. On the nanoscale, the field of quantum computing has surfaced as a powerful model for the development of technology that is very effective in terms of energy consumption. In this article an Energy Efficient QCA based BEC-1 code Converter is proposed. It is designed by employing Feynman Gate and implemented in QCA Designer Tool. By optimizing its layout, BEC-1 has reduced the number of parameters to achieve efficiency, such as the cell count, space occupied in $\mu m^2$, 2.5 clock cycles latency, Average Energy dissipation in meV, Power dissipation in nano watt. According to the findings of the simulation, the proposed design functions without a single glitch and working as per its truth table and exhibits very little energy consumption.**

***Keywords—BEC-1, QCA, Reversible Logic gate, clocking in QCA, QCA designer tool, etc.***

## I. INTRODUCTION

For the purpose of overcoming the constraints imposed by the scalability of Complementary Metal oxide Semiconductor based technology at the nanoscale, QCA is one of the best nanoelectronics technologies that is quickly expanding. It was proposed by ITRS, which stands for the International Technology Roadmap for Semiconductors. There were numerous alternative technologies for CMOS technology that were introduced by the ITRS; but, the QCA has been the most successful nanotechnology up until this point. A significant number of academics and researchers are working towards the actual implementation of QCA circuits in physical world. All QCA circuits are exclusively designed and built using software. Four quantum dots, one for each pair of electrons, make up the square that is the known as QCA Cell. Within the cell, the electrons have a propensity to find and arrange themselves in a diagonal pattern. The electrons undergo vertical shifts, either from the bottom to the top or vice versa, as a result of the tunnelling effect. However, they are unable to travel horizontally, either from the far left to the far right, because of Coulombic repulsion. Those electrons can't possibly be on the identical side due to their equal negative charge, causing them to migrate as

far away from each other as possible. As a result of the electric force acting opposingly on two electrons, two polarisation are created. Electrons located at the left top diagonal positions are denoted by logical value '0' (Polarisation **-1**). If the electrons are located at the bottom left diagonal positions, denoted by logical '1' (Polarisation **+1**). Both the polarization states are shown in Fig. 1. How much space a QCA circuit takes up and how long it takes to complete the process, are two factors that determine circuits cost [1], [2] and it is expressed in equation 1,

$$\text{Circuit cost} = \text{circuit occupancy} * \text{latency}^2 \quad \ldots\ldots\text{equation (1)}$$

## II NOTION OF QCA TECHNOLOGY

QCA based designs are initially created set up in a row of QCA cells, where every cell communicate electronic data to its neighboring cell [3]. The QCA-cell is crucial to the QCA method because it allows computation execution and information transmission within the cells, Bonding configurations involving pairs of electrons are present in every single cell. as depicted in Figure 1.

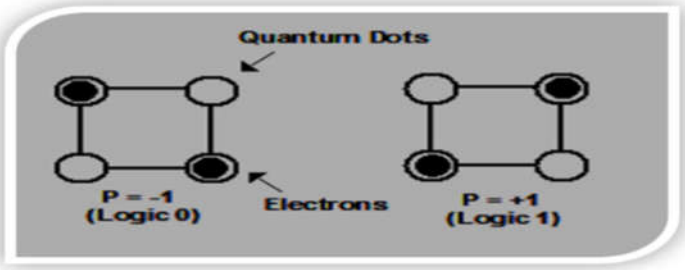


Fig. 1. The phenomenon of polarisation in QCA Cells [4]

Cell polarisation in QCA involves the creation of an electric field within a cell, that decides the binary value of cell either '1' or '0' as per its polrisation. It is possible to obtain QCA cells in two different initial states: the first state is composed of regular cells that are orientated at 90 degrees, and the second state is composed of cells rotated at 45 degrees. A cell with a 90-degree angle is shown in Figure 1 to have a polarization P = 1, is that is equal to 1 in binary [5]. On the other hand, a polarisation state with the value P = -1 is equivalent to the binary value 0. Previous research has shown that cells that are in a relaxed state continue to exist in a state that is not polarised throughout their lifetime [5], [6].

## III CLOCKING IN QCA

The QCA Clocking protocol allows for the creation and invalidation of the metastable stage.[7], [8]. In the QCA clocking action, there are four distinct stages: I-Switch, II-Hold, III-Release, and IV-Relax periods, indicated in Fig.2, When the I-phase (switch) is in progress, walls are raised, and the cells go through a process of polarisation that is

determined by the status of the cell adjacent to them. Barriers are maintained at a high level throughout the II-phase (Hold) so that the outputs can regulate the inputs of the stage. After this, the barriers are reduced during the III-Phase (Release), and the state of the cell becomes neutral. The Relaxed phase is characterised by the cell remaining in a non-polarized state. Four clocking zones, each 90 degrees out of phase with the others, are connected to the cells of a QCA.

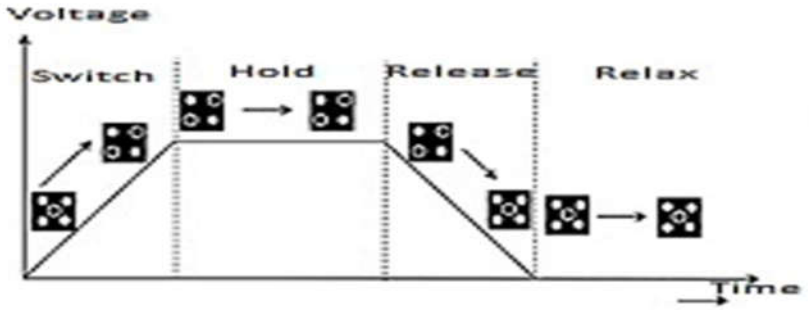


Fig. 2 phases for QCA clocking [4]

## IV ESSENTIAL CONCEPTS ASSOCIATED WITH REVERSIBLE LOGIC

*A.* *Reversible Function-* If there are exactly as many outputs as there are inputs, we say that the Boolean function $F(y_1; y_2,...y_m)$ is reversible. A distinct preimage is associated with each output pattern [9].

*B.* *Reversible Logic*- In reversible logic, a one-to-one mapping can only be established when the number of inputs and the number of outputs of the gates are identical. For each set of input vectors, this method produces a unique set of output vectors. This lessens the impact of data loss, which in turn prevents power from dwindling. Because fan-out is not possible with reversible logic, several outputs cannot be tied to a single input. Additionally, feedback or loops are prohibited in reversible logic circuits. Key features of a reversible logic circuit include:

(1) A limited number of input constants.

(2) Required minimal quantity of reversible gates required.

(3) Optimal Quantity of garbage outputs[9].

*C.* *Garbage Output-* The additional outputs required to provide reversibility in an n-input-k-output function, also known as a (n;k) function, are referred to as garbage. When there is a need to have an equal number of i/p and o/p, more i/p or o/p can be added. The relationship between amount of garbage outputs and constant outputs hasbeen expressed as: “The sum of the input and a constant input equals the sum of the output and the

garbage" [9] .

*D.* *Quantum cost-* known as the cost of the design in relation to the cost of a fundamental gate. It is possible to ascertain the number of fundamental binary reversal gate required to construct the design. Quantum cost is the cost of a circuit that can described using no more than two 2x2 unitary gates while maintaining a constant output. A 2x2 gate incurs the same quantum cost of one as a 1x1 gate, which is 0 [9].

## V REVERSIBLE LOGIC GATE

Reversible logic encompasses three primary design objectives.

1) In order to reduce the device's computational complexity, it is necessary to minimise the quantum cost[10]–[13].

2) The latency, which refers to the extent of complexity in the device, should be reduced to a minimum.

3) The additional i/p and unnecessary o/p that are not part of the gate's design and only exist to ensure the device may be reversed - should be minimized and ideally removed entirely[14], [15].

## VI FEYNMAN REVERSIBLE LOGIC GATE

A Feynman gate is the 2x2 gate, which is known as the controlled NOT gate. This gate is frequently utilized for fan-out reasons. Comprises the inputs (A, B) and the output P=A, Q= A⊕B [16]–[18]. As depicted in Fig 3.

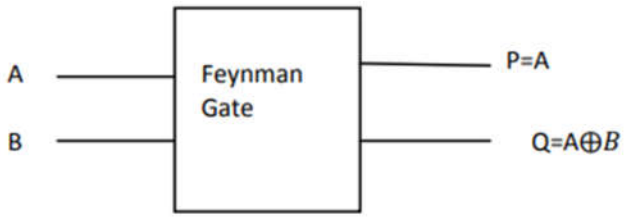


Fig. 3 Feynman Reversible Gate

Truth Table of Feynman Reversible Gate is depicted in fig. 4,

| Input | | Output | |
|---|---|---|---|
| A | B | P | Q |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

Fig.4 Truth Table of Feynman Reversible Gate[18]

## VII BCD TO EXCESS-1 (BEC-1) CODE CONVERTER

BCD to Excess-1 code is very useful for Enhancing the speed of adder Circuit like Carry Select Adder, the main aim of using n-bit BEC-1 is to reduce the delay of addition. Simply adding one binary digit to the converting binary number is all that is needed to transform binary code to excess-1 code. In this case, we solely examined circuits that convert 4-bit binary to excess-1. [2], [19]–[23].

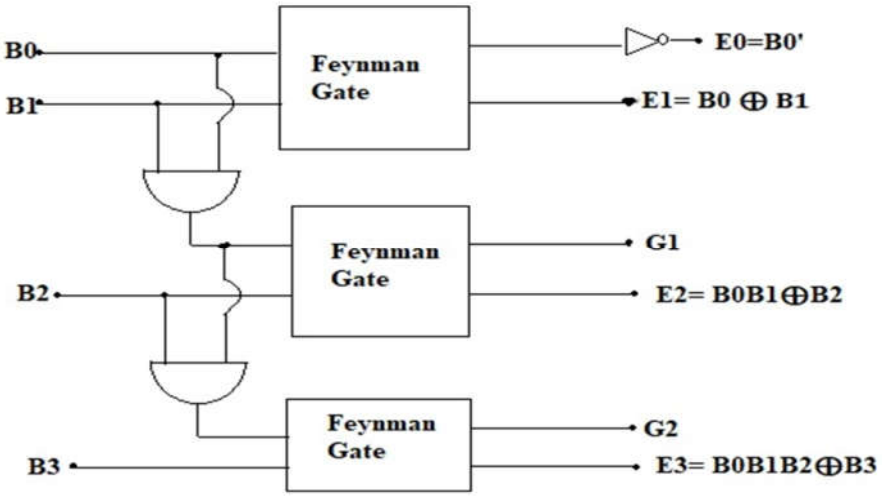


Fig.5. Logic Circuit of Proposed Reversible BEC-1

| B3 | B2 | B1 | B0 | E3 | E2 | E1 | E0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | X | X | X | X |

Fig.6 Truth Table of BEC-1

As shown in Figure 5. Feynman Gate based BEC-1 is a 4x4 combinational Circuit. Its input is B3(MSB), B2, B1 and B0(LSB). The outputs are E3(MSB), E2, E1, and E0(LSB) and there are two Garbage output G1 and G2 as well. The o/p equations of BEC-1 can be written as:

$E3 = B0B1B2 \oplus B3$,

$E2 = B0B1 \oplus B2$,

$E1 = B0 \oplus B1$,

E0 = (B0)’

In this context, the symbol · represents the logical AND operation, the symbol + represents the logical OR operation, and the symbol $\oplus$ represents the logical XOR operation. This circuit has 3 Feynman Reversible Logic gates, one inverter and two AND gates, Figure 5 represent the conceptual diagram of the BEC-1 and Fig.6 shows the truth table of BEC-1 Code Converter.

## VIII IMPLEMENTATION OF PROPOSED BEC-1 USING REVERSIBLE LOGIC GATE IN QCA DESIGNER TOOL

As shown in Fig.7, Proposed BEC-1 using Reversible logic gate is implemented and tested in QCA Designer tool and its functional verification is also done.

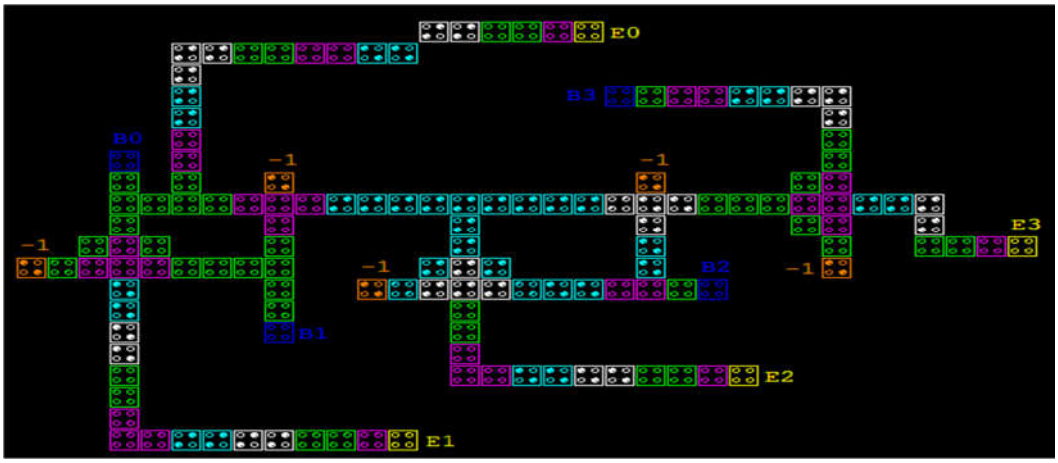


Fig.7 Implementation of Reversible BEC-1 in QCA Designer Tool

## IX RESULT AND SIMULATION WAVE FORM OF IMPLEMENTED BEC-1 CODE CONVERTER

In Figure 8, Simulation waveform of Implemented BCD to Excess-1 Converter is shown, which depicts the functional verification of Implemented design.

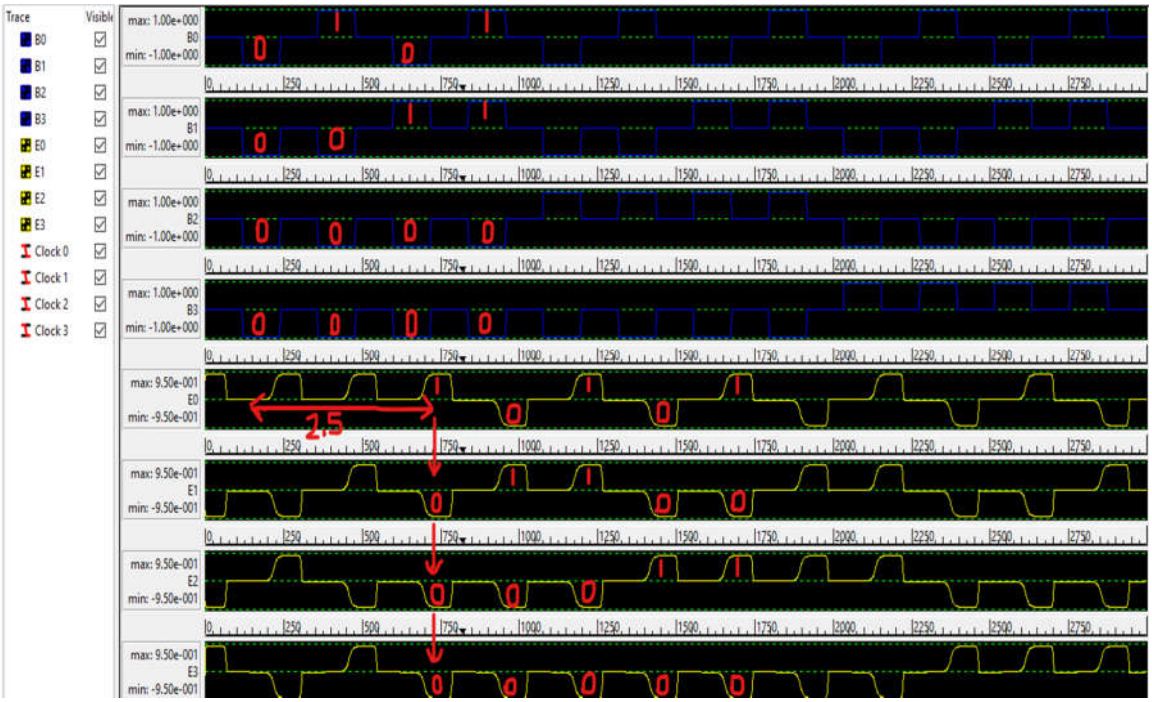


Fig.8 Simulation Output waveform and functional verification of Proposed Reversible BEC-1 Code Converter

Simulation output of implemented BEC-1 Converter is depicted in Table 1.

Table 1. Performance result of Proposed Reversible BEC-1

| Circuit Design | No. of Cells used | Area ($\mu m^2$) | Latency (Clock cycles) | Average Energy Dissipation/cycle Eav | Power Dissipation |
|---|---|---|---|---|---|
| **Proposed BCD to Excess1 (BEC-1)** | **141** | **0.27** | **2.5** | **4.43 meV** | **0.177 nW** |

## VII PERFORMANCE PARAMETERS AND METHODOLOGY USED:

To evaluate the design efficacy of any architecture in QCA technology, five key characteristics must be considered: the number of cells, the area utilized in micrometers square ($m^2$), delay in terms of clock cycles, Average Energy Consumption per cycle and power dissipation. The measuring of these qualities is made easier by the use of a simulation tool known as QCA designer 2.0.3 and QCA Designer E tool [24], [25]. A summary of these and other performance measures is as follows:

1) **Cell count:** The term "cell" refers to the total number of individual components used in the building of a circuit design. The proposed design exhibits a total cell count of 141, as depicted in Figure 7.

2) **Area Occupied:** "Area occupancy" is the measure of how cells are spatially utilized in a circuit. During the design phase, it is standard practice to place each individual cell at a distance of 2 nm from its next cell[4],[26], [27]. Furthermore, it is important to mention that the surface area occupied by a single cell is 324 nm2. The total area is determined by identifying all cells that possess a distinct gap between them. As shown in Figure 7, BEC-1 circuit design collectively occupies an area of 0.27 Micrometer$^2$.

3) **Delay (Latency):** The computation is derived by multiplying 0.25 with the total number of clock phases employed in generating the required output. Proposed BEC-1, seen in Figure 7 employ maximum 10 clock phases to get the desired outcome. Therefore, the latency[28], [29] of the entity is calculated as 0.25 multiplied by 10, resulting in a value of 2.5.

4) **Average Energy Dissipation per Cycles**: Value of Average Energy Dissipation per cycle[30] in proposed design is 4.43 meV.

5) **Power Dissipation:** Value of Power Dissipation[31], [32] in proposed design is 0.177 nW.

## VIII SIMULATION FRAMWORK AND KEY CRITERIA

Simulation Framework and Key Criteria used to realize the circuit are mentioned in table 2.

**Table 2. Simulation Framework and Key Criteria**

| **Parameters/key criteria** | **Values** |
|---|---|
| Radius of effect | 0.065 µm |
| Relative permittivity | 12.9 |
| Cell size | 0.018 µm |
| Cell area | 0.324 $\mu m^2$ |
| Separation gap | 0.002 µm |
| Overall samples | 12000 |
| Convergence tolerance | 0.0000100 |
| Clock low | $3.8x10^{-23}$ J |
| Clock shift | 0 |
| Clock high | $9.8x10^{-22}$ J |
| Clock amplitude factor | 2 |
| Layer Separation | 11.5 |
| Maximum iteration/sample | 100 |

## VII. CONCLUSION AND FUTURE SCOPE

Recent studies examining the development of nano-electronics circuitry have focused on nanotechnology. Since digital logic gates are the fundamental parts of all digital circuits, simpler, faster designs with the fewest possible zones are essential. This paper Proposed an Energy and Area Efficient BEC-1 design, in the QCA Designer tool for nano-scale

applications. The constructed BEC-1 has achieved an optimal layout with less cell count, area occupancy in $\mu m^2$ and delay of only 2.5 clock cycles, average energy dissipation in **meV,** Power dissipation in **nano watt**. According to the execution parameters, the proposed design has the potential to be employed in designing and implementation of QCA based Energy Efficient Fast adders like RCA, CSLA, SQRT CSLA, Binary incrementor circuits to make efficient and speedy ALUs in future.

**Conflicts of Interest-** The Authors declare that they have no conflicts of interest in this work.

**Data Availability**- No data set has been used for this research paper.

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