An Ultra-Low-Power Static Contention-Free 25-Transistor True Single-Phase-Clocked Flip-Flop in 45nm CMOS

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***Abstract*—** Optimizing the power consumption of flip-flops (FFs), as essential components of sequential digital circuits, can significantly reduce the overall energy usage of digital systems. This paper introduces an ultra-low-power true single-phase clocked (TSPC) flip-flop with a 25-transistor design (29 transistors with a reset function). By eliminating redundant charging and discharging and addressing floating nodes through transistor-level optimization, the design achieves a fully static, contention-free operation. Implemented in CMOS technology, demonstrate that the proposed circuit offers exceptionally low energy consumption, making it ideal for energy-efficient applications.

***Keywords*—**CMOS digital Circuits, Flip Flop (FF), Low voltage operation, Ultra-Low-Power, True-Single-Phase-Clock (TSPC)**.**

I. INTRODUCTION

The rapid advancement of processors and the Internet of Things (IoT) has significantly enhanced the performance of digital systems. However, power consumption has become a critical limiting factor for these systems. Flip-flops (FFs), as fundamental components of sequential logic circuits, contribute substantially to the overall power consumption in digital systems. A key issue with traditional FF designs lies in the power consumed by the two-phase clock network, where the clock inverter toggles during every clock cycle. Consequently, minimizing the power consumed by clock signals can effectively reduce the power usage of flip-flops, thereby lowering the total power consumption of the entire digital system.

A flip-flop is a fundamental building block in digital electronics and computer architecture. It is a sequential logic circuit that can store and transfer binary information. Flip-flops are used to create memory elements, registers, counters, and other sequential logic circuits.

A flip-flop operates on clock pulses, which are regular signals that synchronize the operation of digital circuits. The clock signal determines when the flip-flop will store or transfer data. The two most common types of flip-flops are the SR (Set-Reset) flip-flop and the D (Data) flip-flop.

1. SR Flip-Flop:

The SR flip-flop has two inputs, the S (Set) input and the R (Reset) input, and two outputs, the Q output and the $\bar{Q}$ (complement of Q) output. When the S input is activated, the Q output is set to 1, and when the R input is activated, the Q output is reset to 0. The $\bar{Q}$ output is the inverse of the Q output. The SR flip-flop has a potential problem called the "race condition" where both inputs are activated simultaneously, resulting in an undefined state.

2. D Flip-Flop:

The D flip-flop has a single input, the D (Data) input, and two outputs, the Q output and the $\bar{Q}$ (complement of Q) output. The D input determines the state of the Q output. When the clock signal is triggered, the D input is transferred to the Q output. If the D input is high (1), the Q output becomes high, and if the D input is low (0), the Q output becomes low. The $\bar{Q}$ output is the inverse of the Q output.

To address this, several low-power single-phase clocked (TSPC) flip-flops have been developed. However, certain challenges still impact the power efficiency of these designs. For instance, some exhibit high precharge power, while others fail to operate effectively at near-threshold supply voltages. To overcome these issues, an ultra-low power TSPC flip-flop is proposed. The design eliminates redundant precharge operations, significantly reducing power consumption. Additionally, through transistor-level optimization, it achieves fully static and contention-free operation, making it ideal for low-voltage and low-frequency applications.

II. RELATED WORK

The transmission gate flip-flop (TGFF) is the most widely used FF in current digital systems. The schematic of the TGFF is shown in Fig. 1. The TGFF is contention-free and can operate at near-threshold voltages. The primary drawback of the TGFF is its extensive clock network. The internal nodes CKI and CKN are constantly toggling, and each of the two signals has four load transistors, resulting in extreme power consumption.

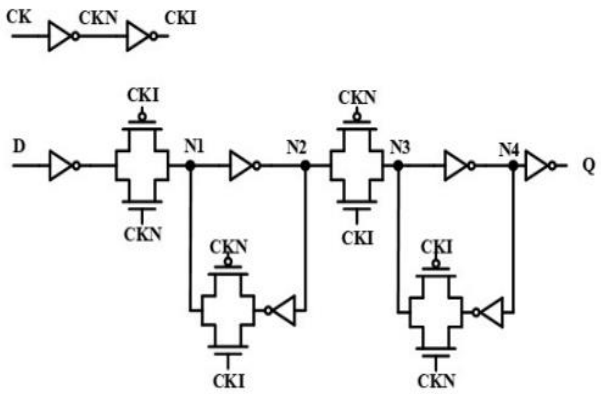

FIGURE 1. Schematic of the TGFF.

The evolution of flip-flop designs for low-power circuits has been driven by the need to reduce power consumption while maintaining functionality. The HFF (High-Frequency Flip-Flop) design, which uses 18 transistors, requires precise transistor width ratios and employs high W/L ratio NMOS transistors for the transmission gate. This setup leads to area overhead and low-voltage disfunction**,** as the design struggles to operate efficiently under low supply voltages.

The SPC-18T FF**,** another low-power flip-flop, faces challenges similar to the S2CFF, particularly the redundant toggling at the internal data node when the data remains at '0', leading to unnecessary power dissipation. Additionally, the hold time issue in the SPC-18T FF causes problems when the input data changes rapidly from '1' to '0', preventing the master latch from fully discharging, which results in functional failure.

The REFF (Redundancy-Eliminated Flip-Flop**)** attempts to address some of these issues by simplifying the inverter phase of the clock signal, generating a new clock signal, CLKB**.** However, this design increases area overhead due to the additional control logic and introduces extra power consumption.

This section provides a detailed description of the structure of the existing flip-flop (FF). As shown in Fig. 2(a), the circuit is composed of 25 transistors. It is important to note that in standard cell libraries, the clock signal of the FF typically includes a clock buffer. This clock buffer is used to balance the clock tree and enhance the clock driving capability of the internal FF circuit. However, for the purpose of this discussion, the clock buffer is omitted because it is a standard component and does not influence the functionality of the FF or the comparisons made below.

During the negative phase of the clock, the input data is transferred to either node L1 or F1, but it does not affect the output data in the slave latch. After the rising edge of the clock, the data is then transferred to the output Q. A PMOS transistor, labeled M11**,** is inserted as the input sense transistor in the recharge path of node F1. It is controlled by the inversion of the input data to prevent charging of node F1 when the input data is '0' during the negative phase of the clock. Without transistor M11, node F1 would be charged to V_{dd} during the negative clock phase and then discharged to GND at the rising edge of the clock, causing unnecessary power consumption. However, when the input data is '1'**,** M11 turns ON, allowing node F1 to be charged to VDD during the negative phase of the clock through the transistors M10 and M11**.** This design helps eliminate redundant power dissipation when the input data is '0'.

Since the insertion of M11, the output data cannot be latched because there is no charge path to node F1 when the clock is low and the output data Q is '1'. To address this issue, a PMOS transistor M12, controlled by L2, is connected in parallel with M11. This ensures that a charge path to node F1 remains available through M10 and M12, allowing M16 to stay ON and create a loop that latches the output data correctly.

The proposed design effectively eliminates potential floating internal nodes, which could otherwise change the correct value due to leakage current. By inserting transistors M6**,** M11, M12**,** M13**,** and M14**,** the internal nodes always maintain a charge path to VDD or a discharge path to GND, regardless of the state of the clock, input data, or output Q, as illustrated by the colored lines in Fig. 2(a). Consequently, the proposed flip-flop achieves a fully static design and can operate correctly across all frequency ranges while consuming very low power.

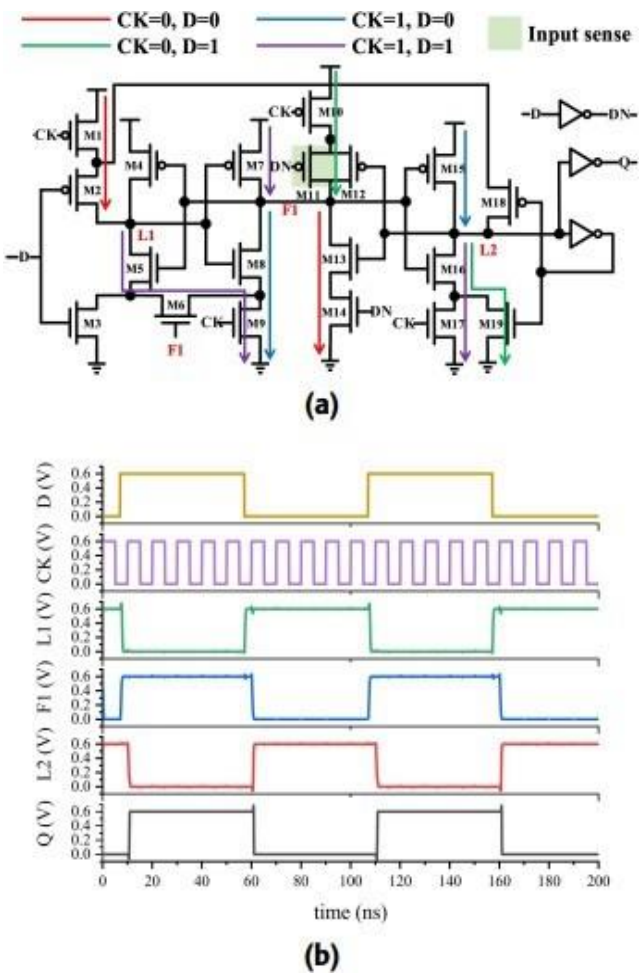

FIGURE 2. (a) Schematic of the existing FF, (b) Transient waveform at 0.6 V.

A. DETAILED OPERATION OF THE FF:

High-to-low Transition:

When the clock (CK) is low and the input data (D) is 0, node L1 is charged to VDD through transistors M1 and M2, and transistor M8 is turned ON. At the rising edge of CK, node F1 is discharged to GND via M8 and M9. Afterward, transistor M15 is turned ON to charge node L2 to VDD, and then the output Q changes to 0 through the inverter.

Low-to-High Transition:

When CK is low and the input data (D) is 1, the signal DN becomes 0. Node F1 is charged to VDD through transistors M10 and M11**.** Simultaneously, the voltage at node F1 keeps transistors M5 and M16 ON. This causes node L1 to discharge to GND through M5 and M3. At the rising edge of CK, node L2 is discharged to GND through M16 and M17, and the output Q changes to 1 through the inverter.

The charge/discharge paths to each internal node consist exclusively of either NMOS or PMOS transistors, ensuring no threshold voltage drop occurs for voltage transfer. This design enables the internal nodes to exhibit a rail-to-rail voltage swing, allowing the proposed flip-flop (FF) to function correctly even at near-threshold voltages. Figure 2(b) shows the transient waveform of the proposed FF at a supply voltage of 0.6 V. As observed in the figure, the internal nodes L1**,** F1, and L2 remain stable when the input data is constant, confirming the stability of the design at low supply voltages.

B. TRANSISTOR LEVEL OPTIMIZATION AND ASYNCHRONOUS RESET:

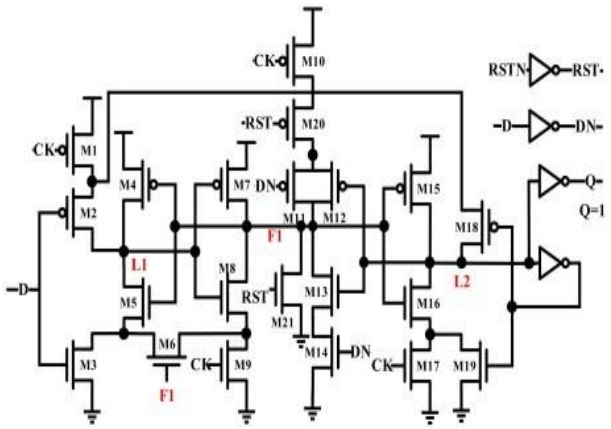

FIGURE 3. Schematic of the existing FF with asynchronous reset.

Fig illustrates the schematic of the proposed flip-flop (FF) with an asynchronous reset function. To achieve this, a pair of transistors M20 and M21 are added to the original design, controlled by the inversion of the reset signal (RSTN).

- When RSTN is high (i.e., RST is low), transistor M20 is ON and M21 is OFF, allowing the circuit to function as previously described, without any modification.
- When RSTN is low (i.e., RST is high), M20 is OFF, blocking the charge path to node F1. Simultaneously, M21 is ON, discharging node F1 to '0'. This triggers M15 to turn ON, which charges node L2 to VDD. Consequently, the output data Q changes to '0', regardless of the input data and clock signal changes, thereby realizing the asynchronous reset functionality.

This design allows the FF to be reset asynchronously, ensuring the output is set to '0' independently of the clock and input data.

III. PROPOSED SYSTEM

A. POWER GATING:

In this topic, the modification in the proposed circuit for FF with asynchronous reset in this design we are going to add the power gating technique to the PMOS. Here, the PMOS is designed using POWER GATING Logic. Here, we also mention the detailed information relating to power gating technique and the advantages towards the modified design.

B. INTRODUCTION TO POWER GATING TECHNIQUE:

Power gating is a technique used in integrated circuits to reduce power consumption by turning off the power supply to specific circuit blocks when they are not needed. This technique is particularly useful in modern chips, which often contain many different functional blocks that may not be used at all times.

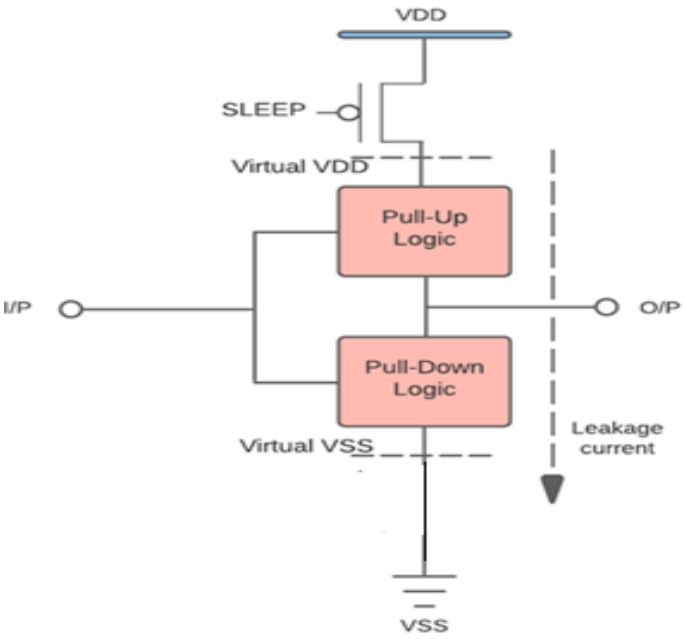

FIGURE 4. Block diagram of Power gating technique.

Power gating works by inserting switches into the power supply paths of specific circuit blocks, which can be controlled by a power management unit. When the circuit block is not needed, the switch is turned off, cutting off the power supply and reducing the power consumption of the circuit.

Power gating is typically used in conjunction with other power management techniques, such as dynamic voltage and frequency scaling (DVFS), to further reduce power consumption in integrated circuits. However, power gating can also introduce some design challenges, such as increased complexity and potential timing issues when switching between power states.

Despite these challenges, power gating is an effective technique for reducing power consumption in integrated circuits and is widely used in many modern electronic devices, such as smartphones, laptops, and other portable electronics.

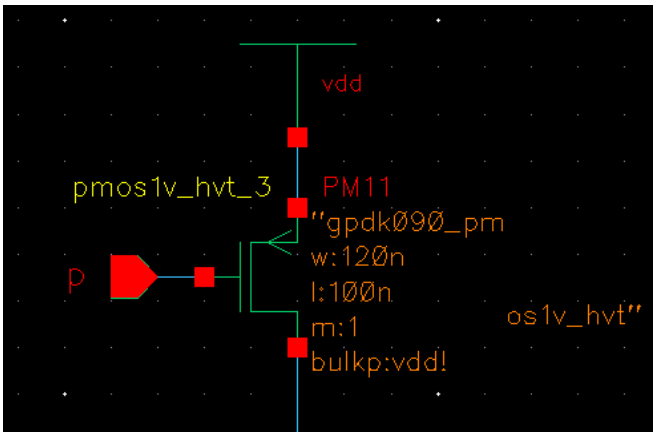

FIGURE 5. PMOS Transistor for Power Gating.

This is the figure5 of the power gating technique we applied in this diagram in previously the V_{dd} supply we are going to applied directly & now coming to extension part we are applying power gating to PMOS transistor & V_{dd} supply via that PMOS transistor, after adding this technique our design power consumption is going to be reduced.

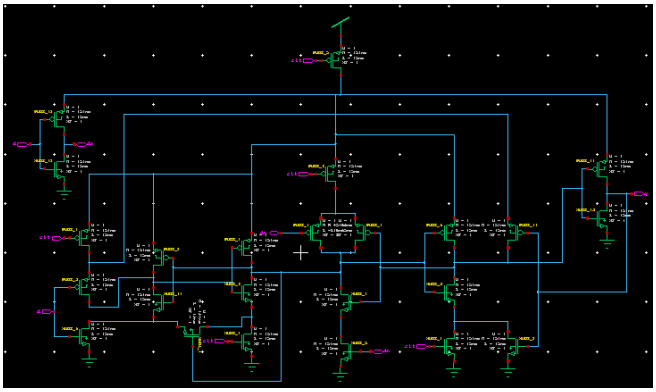

FIGURE 6. The proposed circuit diagram with power gating technique.

The proposed circuit diagram is shown in the adjacent figure6 as we applied low power technique that is power gating logic & the load resistor at the output side, we are going to increase the value of that resistor because of increasing the value gain, compare to exciting method our gain is going to be improved.

IV. SIMULATION RESULTS

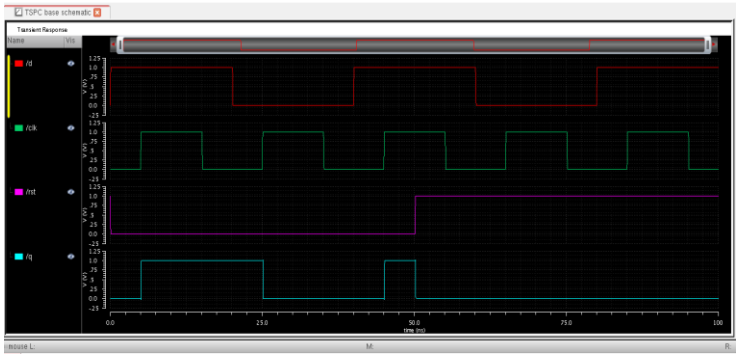

FIGURE 7. Waveform for proposed system

Figure 7 shows the transient waveform of the proposed FF at a supply voltage of 1V.

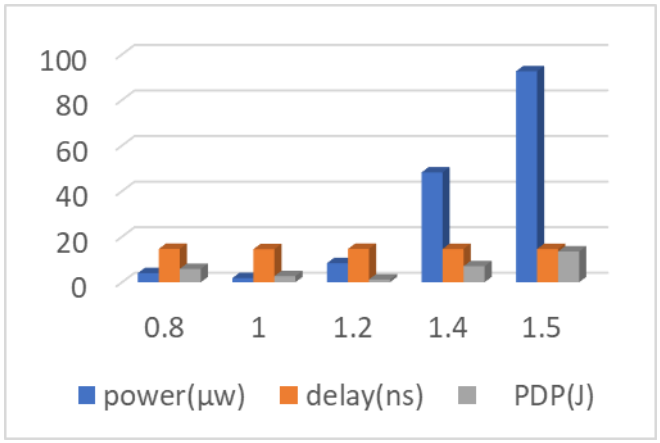

FIGURE 8. Impact of Supply Voltage on Power, Delay and PDP

The figure8 relate to how different voltages affect three parameters in a digital system or circuit: power, delay, and Power-Delay Product (PDP).

A. COMPARISION TABLE:

Metric	Existing @ 55nm	Proposed @ 45nm	Improvement
Power (µW)	3.7467 µW	1.85 µW	50.7%reduction
Delay (ns)	15.413 ns	14.52 ns	5.8% reduction
PDP (fJ)	57.757fJ	26.862fJ	53.5%reduction

Table 1:Comparision of existing and proposed methods

The comparison table 1 presents a performance evaluation between an existing and a proposed design of an ultra-low-power, static contention-free 25-transistor True Single-Phase-Clocked (TSPC) flip-flop. The existing design is implemented using a 55nm CMOS technology, while the proposed design utilizes a more advanced 45nm CMOS technology.

i. Detailed Description of the Table:

The table consists of four columns:

Metric: This column lists the performance metrics being compared. The metrics are:

- Power (µW): Represents the dynamic and static power consumed by the circuit, measured in microwatts.
- Delay (ns): Indicates the propagation delay of the circuit, which is the time it takes for a signal to travel through the critical path, measured in nanoseconds.
- PDP (J): Stands for Power-Delay Product, which is a crucial figure of merit in digital circuit design. It is calculated by multiplying the power consumption by the delay. A lower PDP generally indicates a more energy-efficient design. The unit here is Joules (J), although it's more common to see units like picojoule (pJ) or femtojoule (fJ) given the magnitudes involved. It's possible the 'J' here is a typo and should be a smaller unit prefix.

ii. Analysis of the Results:

The data clearly demonstrates the benefits of moving to a smaller technology node (from 55nm to 45nm). The proposed design at 45nm exhibits significant improvements across all key metrics:

- Power Consumption: The power consumption is reduced by approximately 50.7%. This is a substantial improvement and is a major driving force behind adopting smaller technology nodes, as it leads to lower energy consumption, reduced heat dissipation, and longer battery life in portable devices.
- Delay: The delay is reduced by approximately 5.8%. While this improvement is less dramatic than the power reduction, a decrease in delay translates to higher operating frequencies and thus better performance of the circuit.
- Power-Delay Product (PDP): The PDP, which is a measure of energy efficiency per switching event, shows a significant reduction of approximately 53.5%. This indicates that the proposed design achieves better performance with significantly less energy expenditure.

V. CONCLUSION

The design is an ultra-low power, fully static, contention-free, true single-phase clocked flip-flop with 25 transistors (29 transistors with an asynchronous reset function), optimized for low-voltage and low-frequency digital circuit applications. This flip-flop incorporates only four clock loads, significantly reducing power consumption across a range of supply voltages by eliminating the unnecessary precharging of internal nodes. The design outperforms existing flip-flop configurations by applying power gating technique we can reduce power in terms of power efficiency. Implemented in 45 nm CMOS technology, the measurement results confirm that the proposed flip-flop operates as expected.

VI. REFERENCES

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